GEB Enterprise S.r.l.
General Electronics Business
Via Rocca di Papa, 21 –00179 Roma, Italy
Email: info@geb-enterprise.com - Web: www.geb-enterprise.com

SOPC
System On Programmable Chip

PCI Express: PCIE-15-IO

PCIe

Features

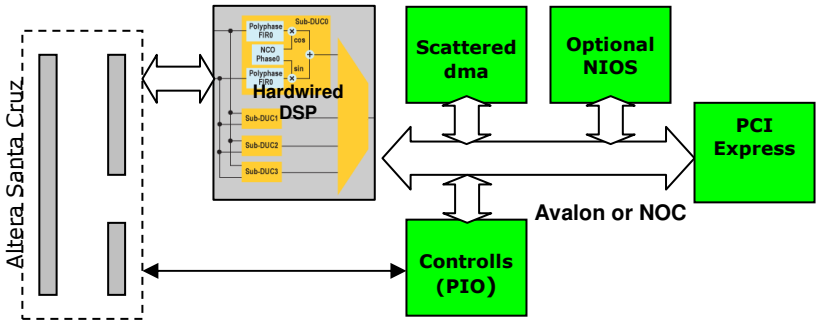
- PCI Express (PCIe) standard size
- Up to 53 user I/O digital channels, 3.3V LVTTL standard, each one with independent sense, drive, bi-directional, and tri-state capabilities.
- Up to 2 user output clocks signals (1 with dedicated PLL), 3.3V LVTTL standard.
- One user input clocks signal, 3.3V LVTTL standard, with dedicated PLL
- Single 3.3 V power supply voltage.
- Connectors (x1):
  - High density, Samtech QSH-030-01-L-DA-RT1 0.5mm pitch on bottom side
  - Medium density, 2X Samtech FTS-1XX-02-F-DV 1,27mm pitch on top sided
  - Altera Santa Cruz connectors set (J11-J12-J13) interface, 3.3 V input tolerant and 3.3V output capable.
  - Low density (100mills) 20pins J14 connector on front panel with 16 I/O, clocks, and wake up signals
- Wake up support
- User available FPGA resources in EP4CGX30 version [*1]:
  - Logic Element: 29440LE (14400LE)
  - Ram: 1080 Kbits (540Kbits)
  - PLL : 4 (3)
  - 18x18 bit multipliers: 80 (none)
- Boot device
- 1 Power supply monitor and reset circuitries.
- One Test Access Ports (TAPs).
- On board crystal oscillator
- Fully-compatible to JTAG/IEEE 1149.1 boundary-scan standard
- Altera USB blaster connector on front panel

(*1) User I/O connectors are available on the top, on the bottom, and on the front side.

Description

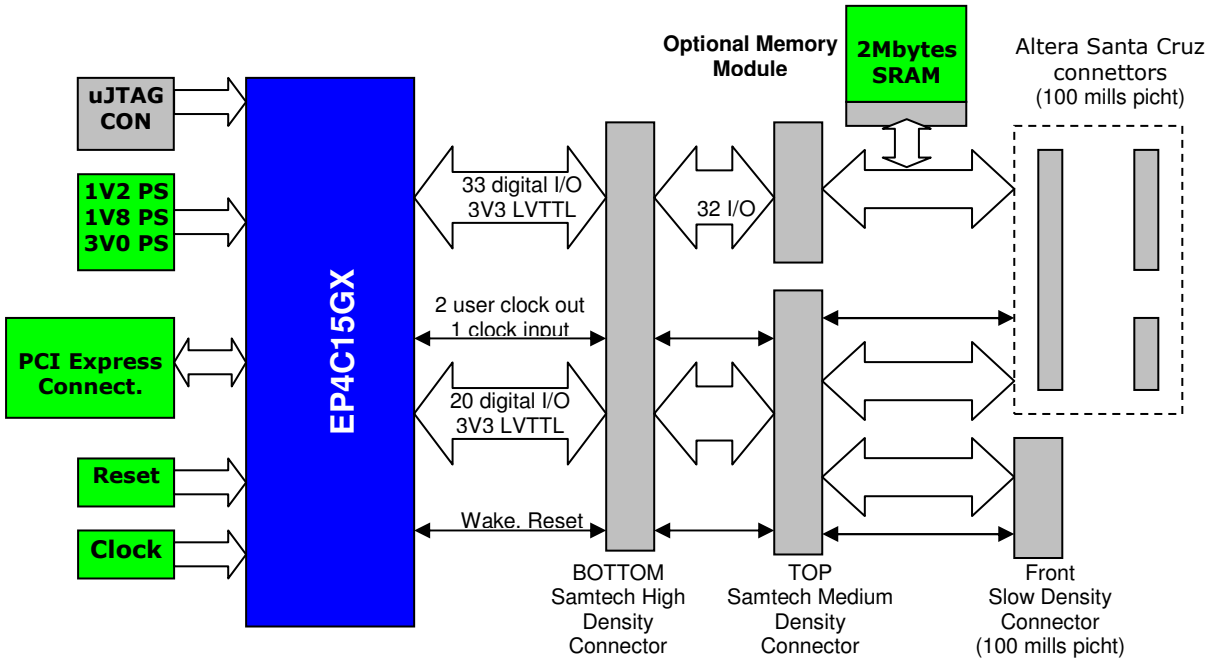
GEB High Performance System On Card (Sopc-Card) product includes, all-in-one, whatever is needed to start using the advanced features of Altera CycloneIV-GX family and features a socketed board with an **EP4CGX15 or EP EP4CGX30**.

All technology FPGA power management, distribution and decoupling, fine pitch package connection, multilayer PCB manufacturing, double side PCB mounting and testing requirements are met by Sopc-Card board. It is also available a programming interface on the board support in-system programming (ISP) using Altera Byte Blaster and JTAG programming and testing.



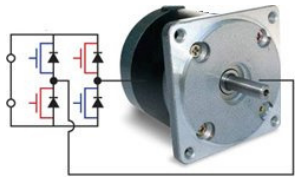
The FPGA hardware design can be easily supported by SOPC builder Altera tools, VHDL language or a combination of them two. Legacy SOPC/QSYS systems may be fitted on all GEB SOPC-PCIe boards family and without any major change. Jungo driver tool fully supports Altera PCIe easy driver development with various Operative Systems, such as Microsoft Windows series, Linux or specific RT/OS.

The expansion connectors allow easy interface with AD/DA or others suitable interface daughter boards (http://www.geb-enterprise.com/files/File/altri_files/Altera_DevTool-Guide_D11.pdf). DSP Builder or SOPC builder, or QSYS builder, allows DSP preprocessing, data management and high speed data transfer from/to host CPU.



Application

A typical application of the product is the control of an I/O sub-system by a standard PC. The flexible and reconfigurable FPGA included in the product allows interfacing to all types of actuators and sensors with, or without, the optional support of the user defined firmware running on a NIOSII core. Moreover, it is also possible implementing in the FPGA a DSP pre-processing, with or without DMA support for data transferring to/from system memory. Moreover, the NIOSII soft core executes custom defined instructions that, together with a very fast interrupts response time (ranging between 1µs and 2µs), allows the user to achieve high demanding processing/time critical requirements, as requested by:.



- Industrial Automation
- Electromedical application
- Electromechanical application
- Fast Data acquisition systems with hardwired integrated Digital Signal Processing
- Led Matrix Control

Specifications and Operating Conditions

Digital I/O levels	Vol = 0.4 V max., Voh = 2.4 V min., Vil = 0.8 V max., Vih = 2.0 V min.
Power supply voltage (current)	3.3 V +/- 5% (0.25A Typical, 0.6A Max) (*2)
Operative temperature range	-40 / + 85 °C
Storage temperature range	-40 / +150 °C

(*2) The current values depends from the configuration file loaded inside FPGA. The typical value was measured on typical application (100MHz system clock, 50% resource usage, 20% I/O switching at 10MHz). Maximum value was estimated using Altera tools in many large and fast designs. The maximum current values allowed depends also from the thermal resistance of the package andfrom the operating temperature

Ordering Information

Product Name	GEB Code	Description
PCIE-15-IO	100815A1	Basic low cost version equipped with EP4CGX15BF14C8N Fpga
PCIE-15-IO	100815A2	Version equipped with EP4CGX30BF14C6N Fpga
PCIE-15-IO	100815A3	Basic low cost version equipped with EP4CGX15BF14C8N Fpga with J2 connectors able to host PCIE-RAM module
PCIE-15-IO	100815A4	Version equipped with EP4CGX30BF14C6N Fpga with J2 connectors able to host PCIE-RAM module
PCIE-RAM	100996A1	2MBytes Memory module

GEB Enterprise S.r.l.
General Electronics Business
Via Rocca di Papa, 21 –00179 Roma, Italy
Phone: 06 7827464 Fax: 06 7806894
Email: info@geb-enterprise.com
Web: www.geb-enterprise.com